

REMARKS/ARGUMENTS

Applicant received the Office Action dated November 19, 2007 in which the Examiner: 1) rejected claims 1–7 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Pat. App. Pub. No. US 2004/0174831 (“Yi”) in view of U.S. Patent No. 6,314,504 (“Dent”) and 2) rejected claims 11, 12 and 19-21 under 35 U.S.C. § 103(a) as being unpatentable over Yi in view of Dent and U.S. Pat. App. Pub. No. US 2004/0002366 (“Cromer”). The Examiner also appears to reject claims 8 and 10 in view of Yi and Dent and to reject claims 13-16 in view of Yi, Dent and Cromer.

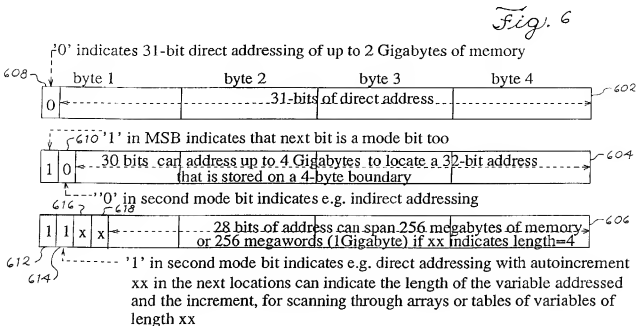
Based on the arguments contained herein, Applicant respectfully requests reconsideration and allowance of the pending claims.

§ 103 REJECTIONS

Appellant respectfully submits that the § 103 rejections of the Office action dated November 19, 2007 are improper. “Any rejection under 35 U.S.C. § 103 must clearly and explicitly articulate the reason(s) why the claimed invention would have been obvious. MPEP § 2142. The framework for determining obviousness under 35 U.S.C. § 103 requires (1) determination of the scope and content of the prior art; (2) assessment of the differences between the claimed invention and the prior art; and (3) assessment of the level of ordinary skill in the pertinent art. MPEP § 2141 (citing KSR International Co. v. Teleflex Inc., 550 U.S. ___, ___, 82 USPQ2d 1385, 1395-97 (2007)). Differences between the claim limitations and the prior art weighs in favor of non-obviousness. To establish obviousness, each of the claim limitations must be taught or suggested by the prior art. See CFMT, Inc. v. YieldUp Int’l Corp., 349 F.3d 1333, 1342 (Fed. Cir. 2003).

With respect to claim 1, the cited references, considered individually or together, fail to teach or suggest “fewer bits are serially transferred between the master device and the slave device for reads and writes in the indirect memory addressing mode than for reads and writes in the direct memory addressing mode.” The Examiner recognizes that Yi fails to even teach direct and indirect addressing modes and cites Dent for teaching these addressing modes. However, Dent still does not teach Applicant’s claimed limitation. Dent’s Figure 6 (reproduced below) explicitly shows that the direct and indirect address modes vary with respect to the number of addressing bits (31, 30 28), but not

with respect to the total number of bits in the read/write instruction (always 32 bits) as the Examiner has already recognized. Office Action dated 11/19/07, page 6, item 5.



Thus, *Dent* does not teach or suggest “fewer bits are serially transferred between the master device and the slave device for reads and writes in the indirect memory addressing mode than for reads and writes in the direct memory addressing mode” as recited in claim 1.

The Examiner argues it would be been obvious to combine *Yi*’s serial communication interface with *Dent*’s addressing modes in order to reduce power consumption. However, as previously explained, *Dent*’s indirect and direct addressing modes do not vary with respect to the total number of bits transferred and thus would not reduce power consumption in a serial interface. Therefore, the proposed combination of *Yi* and *Dent* would not provide the benefit suggested by the Examiner. The Examiner has not addressed these issues and thus has not clearly articulated the reasons why Applicant’s claim 1 would have been obvious in view of *Yi* and *Dent* as is required. For at least these reasons, claim 1 and its dependent claims are allowable.

With respect to claim 8, the cited references, considered individually or together, fail to teach or suggest “the processor and the slave device are configurable to

communicate in multiple modes, each mode being associated with a different read/write command length". The Examiner argues that *Dent's* direct and indirect addressing modes have different command lengths. However, as is recognized by the Examiner (see Office Action dated 11/19/07, page 6, item 5), *Dent's* read/write instructions maintain the same length (32 bits) regardless of the addressing mode. The Examiner cannot simply compare *Dent's* direct and indirect address fields to Applicant's claimed read/write commands because Applicant's read/write commands clearly involve more than simply an address length (*i.e.*, each command comprises "a read/write field, a data length field, and an address field" as recited in claim 8). Thus, *Dent* does not teach or suggest Applicant's claimed "different read/write command lengths" as in claim 8. For at least these reasons, claim 8 and its dependent claims are allowable over *Yi* and *Dent*.

With respect to claim 13, the cited references, considered individually or together, fail to teach or suggest "configuring the device to interpret read/write commands having a reduced length if the power consumption parameter exists." For much the same reasons as given previously with respect to claim 1, *Dent* does not teach read/write command having a reduced length as is argued by the Examiner. Office Action dated 11/19/07, page 5, paragraph 1.

The Examiner argues it would be been obvious to combine *Yi*, *Dent*, and *Cromer* because *Dent's* indirect addressing mode would enable *Cromer's* mobile device to consume less power when operating on battery power. However, as previously explained, *Dent's* indirect and direct addressing modes do not vary with respect to the total number of bits transferred and thus would not reduce power consumption in a serial interface. Therefore, the proposed combination of *Yi*, *Dent*, and *Cromer*, would not provide the benefit suggested by the Examiner. The Examiner has not addressed these issues and thus has not clearly articulated the reasons why Applicant's claim 13 would have been obvious in view of *Yi*, *Dent*, and *Cromer* as is required. For at least these reasons, claim 13 and its dependent claims are allowable.

With respect to claim 19, the cited references, considered individually or together, fail to teach or suggest "means for conveying a "not busy" signal from the slave device to the master device during the first and second modes, the "not busy" signal having fewer

bits in the second mode than in the first mode.” The Examiner appears to argue that *Yi* teaches Applicant’s claimed “not busy” signal limitations at page 1, paragraph 11. Office Action dated 11/19/07, page 6, paragraph 1. Applicants do not find in *Yi*’s paragraph 11 a teaching of a “not busy” signal and much less a teaching of a “not busy” signal having fewer bits in a second mode than in a first mode as recited in claim 19. The Examiner has not clearly articulated why Applicant’s claimed “not busy” signal limitations would have been obvious in view of *Yi*, *Dent*, and *Cromer*. For at least these reasons, claim 19 and its dependent claims are allowable.

CONCLUSION

In the course of the foregoing discussions, Applicants may have at times referred to claim limitations in shorthand fashion, or may have focused on a particular claim element. This discussion should not be interpreted to mean that the other limitations can be ignored or dismissed. The claims must be viewed as a whole, and each limitation of the claims must be considered when determining the patentability of the claims. Moreover, it should be understood that there may be other distinctions between the claims and the cited art which have yet to be raised, but which may be raised in the future.

Applicant respectfully requests reconsideration and that a timely Notice of Allowance be issued in this case. Applicant hereby petitions for any time extensions that are necessary to prevent this case from being abandoned. In the event that additional fees related to this Amendment, or other transactions in this case, are required (including fees for net addition of claims and for time extension), the Examiner is authorized to charge Texas Instruments Incorporated’s Deposit Account No. 20-0668 for such fees.

Respectfully submitted,

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